Abstract of the Disclosure

A pipeline memory device including a data fetching control circuit and utilizes a data fetching method. The pipeline memory device includes a first, second, and third pipeline stages. A second pipeline control signal, for operating the second pipeline stage, is generated from a first pipeline control signal. The data fetching control circuit includes the following: A first edge trigger delay circuit that receives the clock signal for generating the first pipeline control signal and generates the first pipeline control signal. A second edge trigger delay circuit that receives the clock signal for generating the first pipeline control signal. A first inverter that inverts the first pipeline control signal. A NAND gate that inputs the outputs of the first inverter and the second edge trigger delay circuit. A second inverter that inverts the output of the NAND gate to output the second pipeline control signal. A time margin between the first pipeline control signal and the second pipeline control signal can be broadened for high-frequency operation because the second pipeline control signal is activated depending on the point of activation of the first pipeline control signal.